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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PORTKA, GARY J	

ART UNIT	PAPER NUMBER
2188	13

DATE MAILED: 02/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/822,643	FANNING, BLAISE B.	
	Examiner	Art Unit	
	Gary J Portka	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1, 4, 14, 17, 27, and 30 have been amended by Applicant. Claims 1-32 are pending.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 1 recites "a chipset cache controller coupled to the processor cache unit internally to the processor", which is vague and indefinite because it is unclear whether "internally" refers to the chipset cache controller or just to the coupling; in fact, it appears more likely that it refers only to the coupling since "internally" is an adverb which modifies the verb "coupled". In claim 14, the term "internally" appears to modify "controlling", and not necessarily the controller. It is suggested to amend to show "chipset cache controller internal to the processor" (in both claims 1 and 14 change "internally" to "internal", in claim 1 additionally move "internal to the processor" to be after "chipset cache controller". All other claims that depend from these (2-13 and 15-26) are rejected for the same reasons.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented

and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 14-15, and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al., U.S. Patent 6,237,064 B1, in view of Cho, U.S. Patent 6,629,218 B2, and further in view of Lentz et al., U.S. Patent 6,047,348.

6. As to claims 1-2, 14-15, and 27-28, Kumar discloses the recited apparatus, method, and system including processor with cache unit (L1) and internal controller for external chipset cache (L2) with tag store and coherency controller, see Abstract, Figure 1, column 3 lines 9-30 and column 3 line 63 to column 4 line 13, and column 4 line 66 to column 5 line 6. Kumar does not disclose that the L2 cache is part of a memory controller. However, it was known that such an L2 cache could be placed either separately (on a back side bus as depicted in Kumar), or on the same bus with the memory controller (see Cho, Fig. 1). Cho further notes that for specific preferences any configuration or combination of integrated circuits may be implemented (see col. 5 lines 38-46), and therefore it is clear that the L2 cache 14 may be integrated with the memory controller 16 if desired. This would achieve any number of recognized advantages such as reduced cost by using available parts, or by reducing the number of separate parts needed. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to include the L2 cache in a memory controller, because it was known that an L2 cache could advantageously be implemented adjacent to a memory controller in such a system, and integration of such parts was well known and was taught by Cho.

Neither Kumar nor Cho teach double or quad-pumped control signals. However, such signals were well known and commonly used in the art. Lentz teaches that double-pumping reduces the number of bit lines required for a bus. Thus it would have been obvious to one of ordinary skill in the art at the time of the inventio to use double or quad-pumped signals, because this was known to reduce bit line requirements and therefore reduce cost.

7. Claims 3-13, 16-26, and 29-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al., U.S. Patent 6,237,064 B1, in view of Cho, U.S. Patent 6,629,218 B2, further in view of Lentz et al., U.S. Patent 6,047,348, and further in view of Gilda, U.S. Patent 6,438,657 B1.

8. As to claims 3, 16, and 29, neither Kumar, Cho, nor Lentz disclose the coherency protocol is MESI. However, this was a well known and common coherency protocol known at the time, and was known to be specifically beneficial to a system having on-chip L1 and on-chip controller for L2, as taught by Gilda (see Figure 1, and column 11 line 52 to column 12 line 24); therefore an artisan would have been motivated to use MESI in Kumar. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to use a MESI protocol, because it was a well known coherency protocol and was previously taught in analogous devices.

9. As to claims 4-13, 17-26, and 30-32, the recited signals, indicators, and resulting operations are disclosed or inherent to the operation of Kumar, or as taught in Gilda are indigenous to the coherency operations involving multi-level caches, and as such would

have been obvious to provide in Kumar as a function of providing the MESI protocol as described above.

Response to Arguments

10. Applicant's arguments filed January 20, 2004 have been fully considered but they are not persuasive. Applicants argue that the references alone or in combination do not disclose controlling cache memory in an external chipset. Examiner disagrees since Kumar discloses control of an external cache die (L2) via on-CPU chip tag array/queue. If the argument is intended to incorporate a definition of "chipset" as including both a cache and a memory controller, Examiner still disagrees since a teaching (Cho) and motivation was shown for integrating these.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gary J Portka whose telephone number is (703) 305-4033. The examiner can normally be reached on M-F 9:30 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 305-3900.

Gary J Portka
Primary Examiner
Art Unit 2188

February 9, 2004